A 150nW 32 kHz mobility-compensated relaxation oscillator with +/-30ppm/ºC temperature stability

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***Abstract*— A relaxation oscillator is presented that makes use of a current-mode Schmitt trigger to reduce the effects of process, voltage and temperature (PVT) variations. A detailed analysis of the oscillator, including the temperature performance, is presented and verified by experimental results. A test chip with a typical frequency of 32 kHz was fabricated in a 0.18 µm standard CMOS process. The measured frequency variations were +/- 30 ppm/ºC for temperature variation from -20 ºC to 80ºC and +/- 500 ppm/V for supply voltage variation from 0.7 V to 1.8 V. The short term stability is 66 ppm (2 ns) of jitter while the long term stability is 500 ppm of Allan deviation after 10 seconds. A careful design results in a total area of 0.1 mm^2 and a power consumption of 150 nW.**

***Keywords*— Current comparator; Current-mode Schmitt trigger; Low power design; Power management; Relaxation oscillator; Zero-Vt MOSFET**

I. INTRODUCTION

In order to maximize the battery life in power management systems [1], for applications such as heart rate monitors, blood glucose meters, or pacemakers; a low power clock generator with good long term stability is required. Such devices are in standby mode most of the time and wake up at regular short time intervals to perform measurements. The standby mode must be very low in consumption in order not to become the dominant energy consumer. At the same time, the clock generator used for power management has to be stable over time, and the integration of this clock with other functions is generally required.

For this purpose a low power Relaxation Oscillator (RO) is a good candidate [1]. The conventional RC oscillator is the most designed RO, but it has technology limitations, *i.e.* the stability of the oscillator frequency is dependent on both the resistors available in the technology and on the supply voltage. Insensitivity with supply voltage can be achieved through the use of a local low-drop-out regulator [2]. Stability with temperature can be attained by using series-parallel combination of resistors [3], with positive and negative temperature coefficients. However, the temperature coefficient of resistors can vary from batch to batch, which makes the cancellation of the overall temperature coefficient a difficult task. Some recent publications report relaxation oscillators based on the mobility of the MOSFET [4], [5]. This kind of oscillator is a new approach which allows the design of stable relaxation oscillators that do not use resistors. In [4], a low power mobility-based time reference is shown, but the global variation of the oscillation frequency with respect to process, voltage and temperature (PVT)is higher than 1 % without trim-ming. In [5], another mobility-dependent relaxation oscill-ator is presented with power consumption around 41 µW but it has a global variation greater than 0.5% without trimming. In this work we present a new topology of relaxation oscillator based on mobility, which is capable to achieve higher precision and lower power dissipation than those reported in previous papers.

This paper is divided into two sections. In Section II we present the new mobility-compensated relaxation oscillator and in Section III test and measurement results are shown.

II. MOBILITY-COMPENSATED RELAXATION OSCILLATOR

Fig. 1 shows the block diagram of the proposed oscillator. The relaxation oscillator is divided into three blocks: 1. A zero-Vt self-biased current source (zero-Vt SBCS), which is, in fact, a specific current extractor of a zero-Vt transistor. 2. A voltage-controlled current source (VCCS). 3. A current-mode Schmitt trigger (CMST).

The oscillator of Fig. 1 works as follows. Suppose, initially, that the output of the current-mode Schmitt trigger (CMST) is high. In this case, the current through S_1 is zero and the current through S_2 is I_1+I_2. Thus, the capacitor-connected transistor is charged by the current I_1+I_2, and the voltage across it increases, as shown in Fig. 2. The constant K is calculated to make $KI_1 > I_2$; thus, when the output of the CMST is low the discharging current of the capacitor is $K.I_1-I_2$.

As is clear from Fig. 2, the capacitor charging (T_1) and discharging times (T_2) are

$$T_1 = \frac{C_{mos}V_h}{I_1+I_2} \quad T_2 = \frac{C_{mos}V_h}{KI_1-I_2} \tag{1}$$

As shown in Fig. 3, the capacitor voltage is converted into a current I_C through a zero-Vt MOSFET used as a resistor in the VCCS. A copy of this current is then compared to I_1+I_2 or I_2 in the CMST using a current comparator. When $I_c > I_1+I_2$ the output of the CMST switches from high to low, making the current through S_1 to switch from 0 to $K.I_1$ and the current of S_2 to switch from I_1+I_2 to I_2 and the MOS capacitor to discharge.

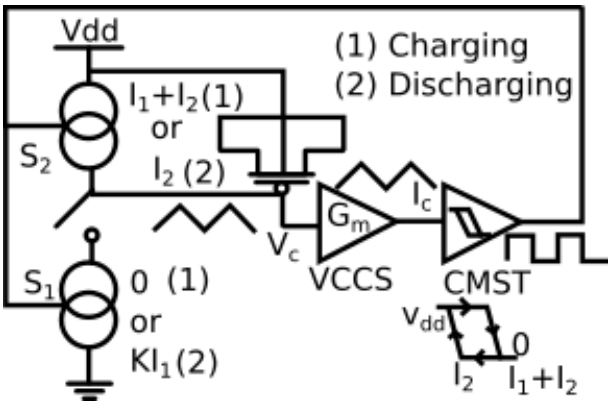

Fig. 1. Diagram of the proposed relaxation oscillator.

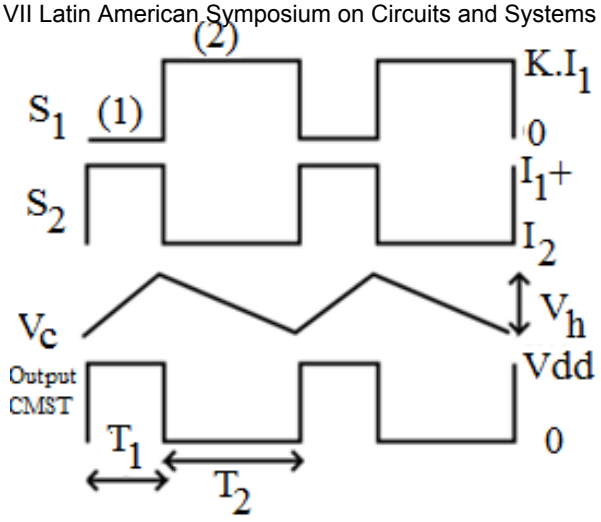

Fig. 2. Waveform of the proposed relaxation oscillator.

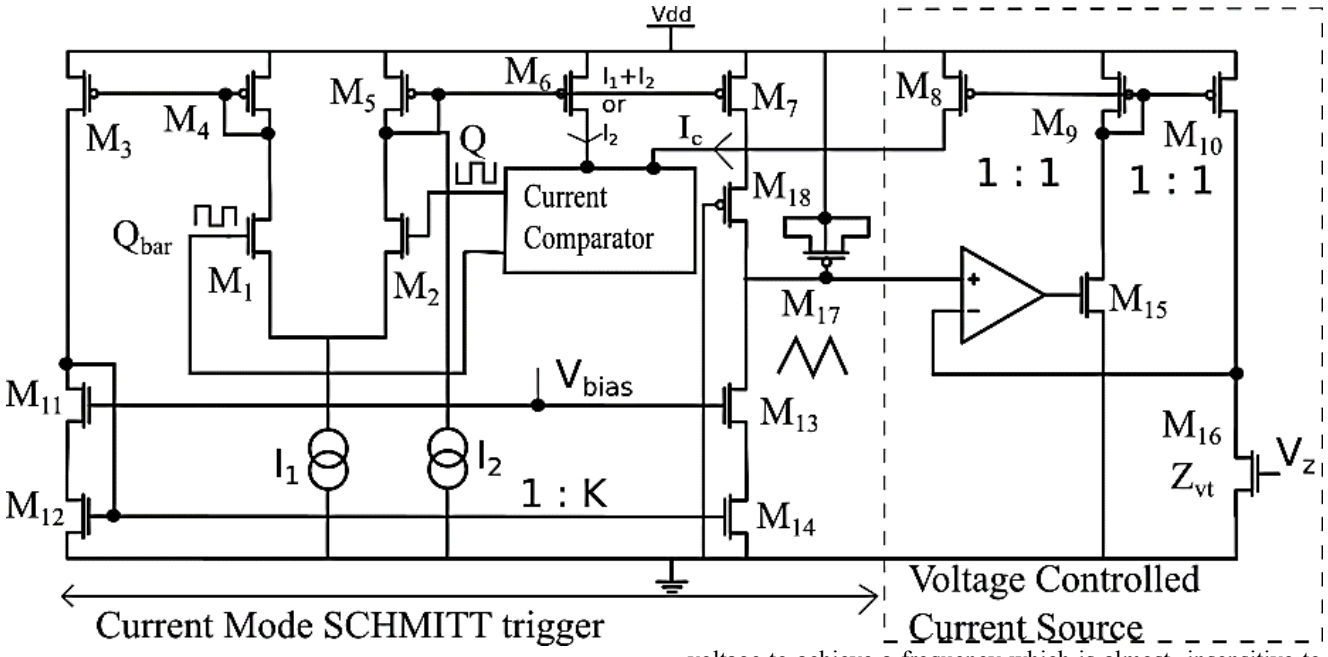

Fig. 3. Full schematic of the proposed relaxation oscillator.

When the current $I_c < I_2$, the output of the CMST goes from low to high and the capacitor is charged once again by the current $I_1 + I_2$. Thus, the swing of the current I_C is I_1, and consequently the hysteresis width of the voltage on the capacitor C_{mos} is

$$V_h = \frac{I_1}{g_{md16}} \tag{2}$$

Since the voltage hysteresis width is proportional to the charging current, any variation in the current reference due to process, voltage and temperature (PVT) affects the hysteresis voltage and the charging (discharging) current in the same proportion; thus, the charging and discharging times are not affected. From (1) and (2), we obtain the oscillation frequency (Hz) as shown in (3)

$$f_0 = \frac{1}{T_1 + T_2} = A\mu_n\phi_t \tag{3}$$

where $A=\frac{(K-1)(1+K_1)(\sqrt{1+i_{r16}}-1)}{(K+1).L^2}$ and I_1, I_2 are copies of the same current reference, $K_I = I_2/I_1$, K is a currrent ratio, i_{r16} is the reverse inversion level of the zero-Vt MOSFET M_{16}, which in this case, is constant [8]. In our approach, the oscillation frequency is proportional to an RC_{mos} product, where R is the zero-Vt resistance and C_{mos} is the MOSFET gate capacitance. Since R is inversely proportional to the oxide capacitance C_{ox} and C is proportional to C_{ox}, the time constant is independent of C_{ox}.

The dependence of the mobility with temperature is $\mu_n = \mu_0 (T/T_0)^{-\alpha}$ [6], where $1.2 < \alpha < 1.8$. At low doping level, which is the case of the zero-Vt MOSFET, $\alpha \approx 1$. This is another reason for using a zero-Vt MOSFET as a resistor; this way, the mobility variation with temperature compensates the thermal voltage to achieve a frequency which is almost insensitive to temperature variation, as given by (3).

Fig. 4 shows the full schematic of the zero-Vt SBCS based on the circuit of reference [8], with zero-Vt transistors M_1 and M_2. Contrary to the standard transistor in the Self-Cascode MOSFET [8], in which the short circuit between drain and gate generally ensures that the device operates in saturation, the diode connection in the zero-Vt transistor does not ensure operation in saturation. In order to bias the zero-Vt transistor in saturation, we have included a diode-connected, standard MOSFET Mn1, biased by a constant current-source Mn2, in order to produce a voltage drop between the drain and the gate of the zero-Vt. The voltage node V_y is designed in such a way to allow $V_y - V_x > V_{dsat2}$, where V_{dsat2} is the minimum saturation voltage of the transistor M_2 in Fig. 4, and $V_x = \phi_t.\ln(J.K_0)$ [8]. The relashionship between the inversion levels of transistors M_1 and M_2 in Fig. 4 is given by $i_{f2}\left[(S_2.(N-K_c+1)/S_1(N-K_c)\right)+1] = i_{f1}$ where N, K_c, K_0 and J are constant. $S_1 = W_1/L_1$ and $S_2 = W_2/L_2$ are the aspect ratio of transistors M_1 and M_2, respectively. As transistor M_2 in Fig.4 is in saturation, the current reference $I_{ref} = I_{SH} S_2 i_{f2}/(N-K_c)$; $I_{SH} = n.\mu_n C'_{ox} \phi_t^2/2$ is the normalized specific current.

All zero-Vt MOSFET used in this design are biased by the same gate voltage V_z, then any change in a zero-Vt MOSFET, results in the same change in the zero-Vt SBCS and the VCCS. The non-linearities of the resistor and the capacitor are limiting factors in the design of the relaxation oscillator. The capacitor voltage should be designed in such a way to allow transistors M_{13} and M_{14} in Fig. 3 to remain in saturation, while keeping M_{16} in the triode region. The non-linear capacitor M_{17}, in turn, operates in the strong inversion region, as shown in Fig. 5.

In order to keep the MOSFET capacitor M_{17} (Fig. 3) in the strong inversion region for a wide supply voltage range, we biased the bulk of the MOSFET capacitor with the supply voltage. The circuit shown in Fig. 6, which is a modified topology of the simple current comparator reported in [10], has been used in the current mode Schmitt trigger of this work.

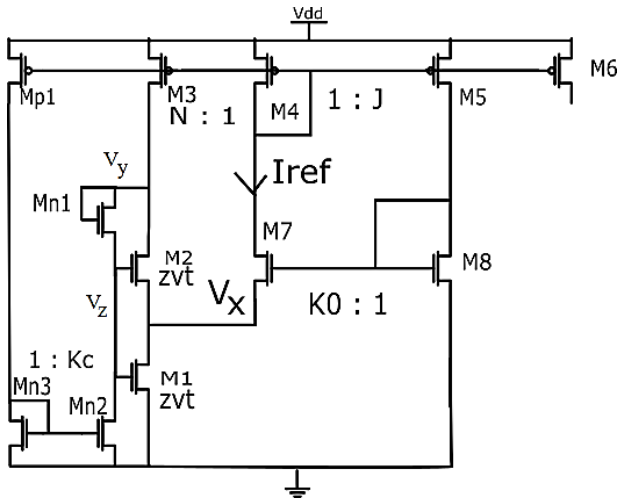

Fig. 4. Zero-Vt self-biased current source.

III. Measurement Results

The oscillator was fabricated in a 180 nm CMOS process and generates a 32 kHz frequency. The die photo of the fabricated relaxation oscillator is shown in Fig. 7. The total area of the oscillator is 0.1 mm^2.

The die contains 8 oscillators with the same nominal frequency, but located at different positions, with the goal to determine variations in same die. The oscillator operates from 0.7 V to 1.8 V; the currents I_1 and I_2 are respectively 24 nA and 36 nA and the total power consumed by the oscillator is 150 nW. The current reference generates 12 nA from VDD in the range from 0.7 V to 1.8V. In this range, the proposed relaxation oscillator has a frequency variation of less than 500ppm/V. Fig. 8, shows the output waveform of a sample of the fabricated relaxation oscillators.

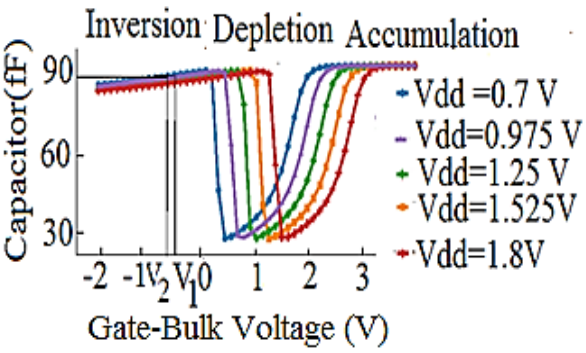

Fig. 5. Simulation result of the operating region of the p-MOSFET as capacitor at different supply voltage. V_1 and V_2 represent the range of operation of the capacitor voltage when the supply voltage is 0.7 V.

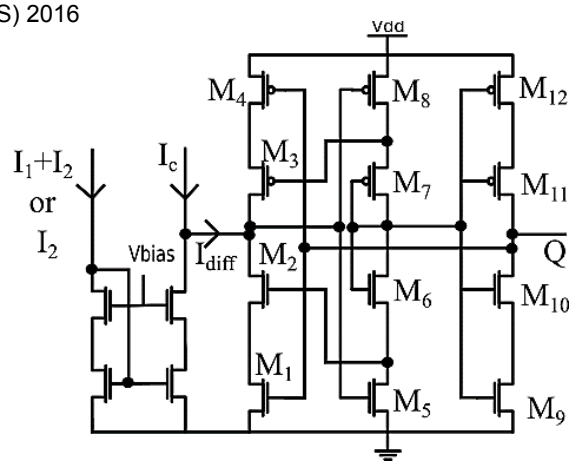

Fig. 6. Schematic of the current comparator.

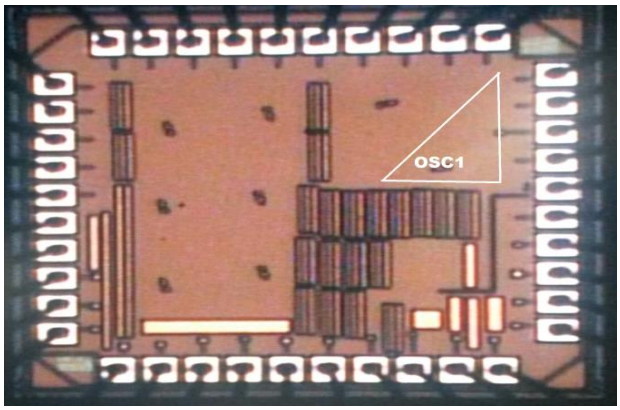

Fig. 7. Die photo of the proposed relaxation oscillator.

To assess the frequency variation with temperature, 5 different oscillators from different dies have been tested with respect to temperature. In the range of -20ºC to 80ºC, the oscillators have an average frequency variation of 30ppm/ºC. As regards the supply voltage variation, we have obtained a variation in the range 500ppm/V to 7000 ppm/V for 8 different oscillators in the same die. The short term stability of the oscillator has been assessed by measuring the jitter, which has achieved 66 ppm, or equivalently 2 ns .

The long term stability of the oscillator is also critical to sleep mode timer performance, and is captured by the Allan deviation, plotted in Fig. 9 for a measurement in a typical office environment. At an averaging time of 10 ms, we have the white noise process limited to 500ppm; and beyond this, it is flicker noise process limited. Table.1 shows a comparison between the proposed relaxation oscillator and some results reported in literature.

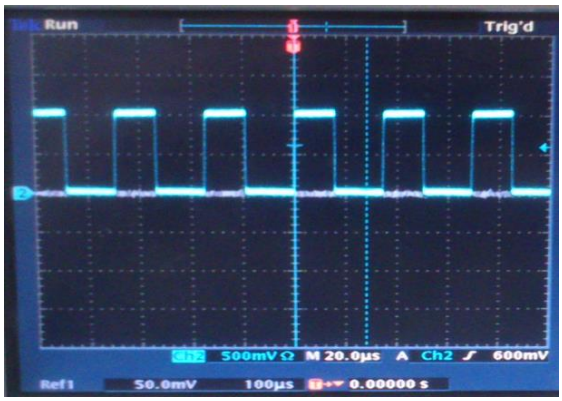

Fig. 8. Output waveform of the relaxation oscillator.

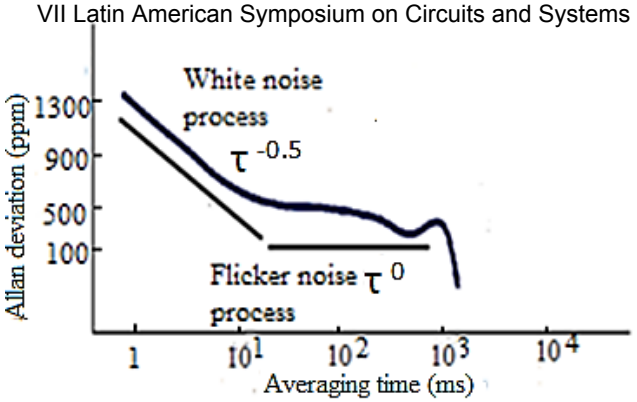

Fig. 9. Allan deviation plot over 24 hours.

TABLE.I: SUMMARY OF MEASURED RESULTS AND COMPARISON WITH PREVIOUS WORKS (NI: NOT INFORMED).

Ref.	[2] ISSCC´14	[4] TCAS´10	[5] ESSCIRC 08	[9] ISSCC´13	This work
Process (nm)	65	350	65	65	180
Area (mm^2)	0.015	0.1	0.11	0.032	0.1
Freq (kHz)	33	3.3	100	18.5	32
Power (nW)	190	11	41000	120	150
Temp Accuracy %	+/-0.21	> 1	> 0.5	+/-0.25	+/- 0.3
Temp range ºC	-20 to 90	-20 to 80	-22 to 85	-40 to 90	-20 to 80
Voltage Accuracy	0.09 %/V	3.5 %/V	0.1 %/V	1 %/V	0.05 %/V
Allan Deviation (ppm)	< 4	NI	NI	<20	500
Jitter (ppm)	NI	NI	NI	NI	66

IV. CONCLUSIONS

The employment of an oscillator topology in which the hysteresis width and the the charging/discharging current are proportional to each other allows for a current insensitive oscillation frequency. The use of a zero-Vt transistor as a resistor allows for a compensation of the thermal voltage, thus leading to an oscillator almost insensitive to temperature.

Summarizing, a mobility-compensated time reference using zero-Vt MOSFET as resistor and PMOS transistor as a capacitor was able to achieve an average frequency variation of 30 ppm/ºC and a minimum 500 ppm/V supply voltage sensitivity. A long term stability of 500 ppm after 10 seconds and a short term stability of 66 ppm of jitter have been achieved.

ACKNOWLEDGMENT

The authors would like to express gratitude to MOSIS for fabricating the circuit, under the MEP research program and to CNPq. Also the authors would like to express gratitude to Prof. Adroaldo Raizer for his help with the noise measurements.

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